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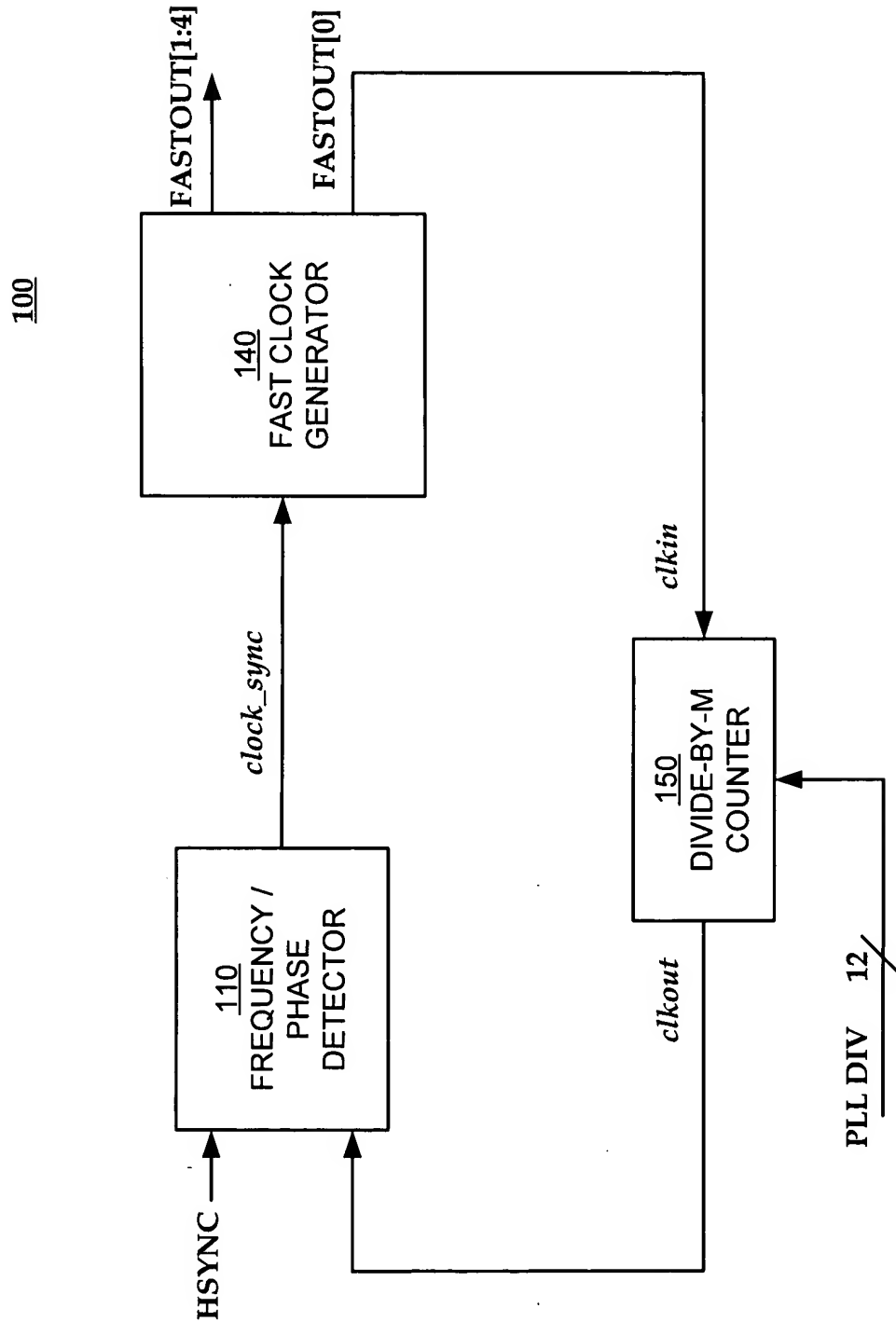


FIGURE 1

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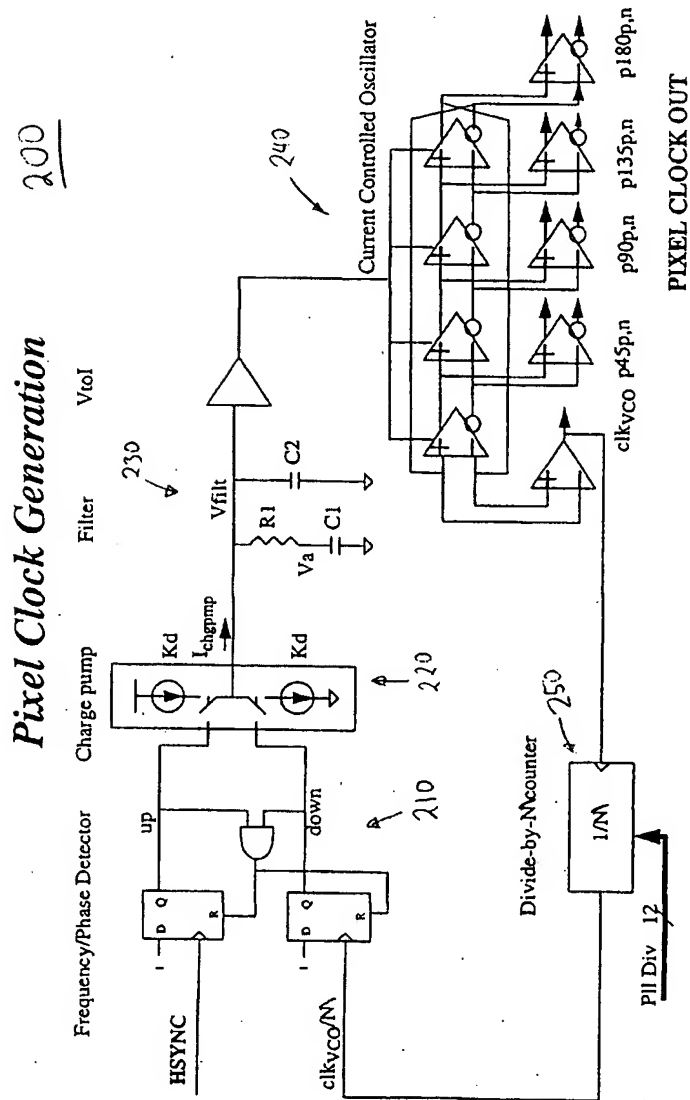


FIGURE 2

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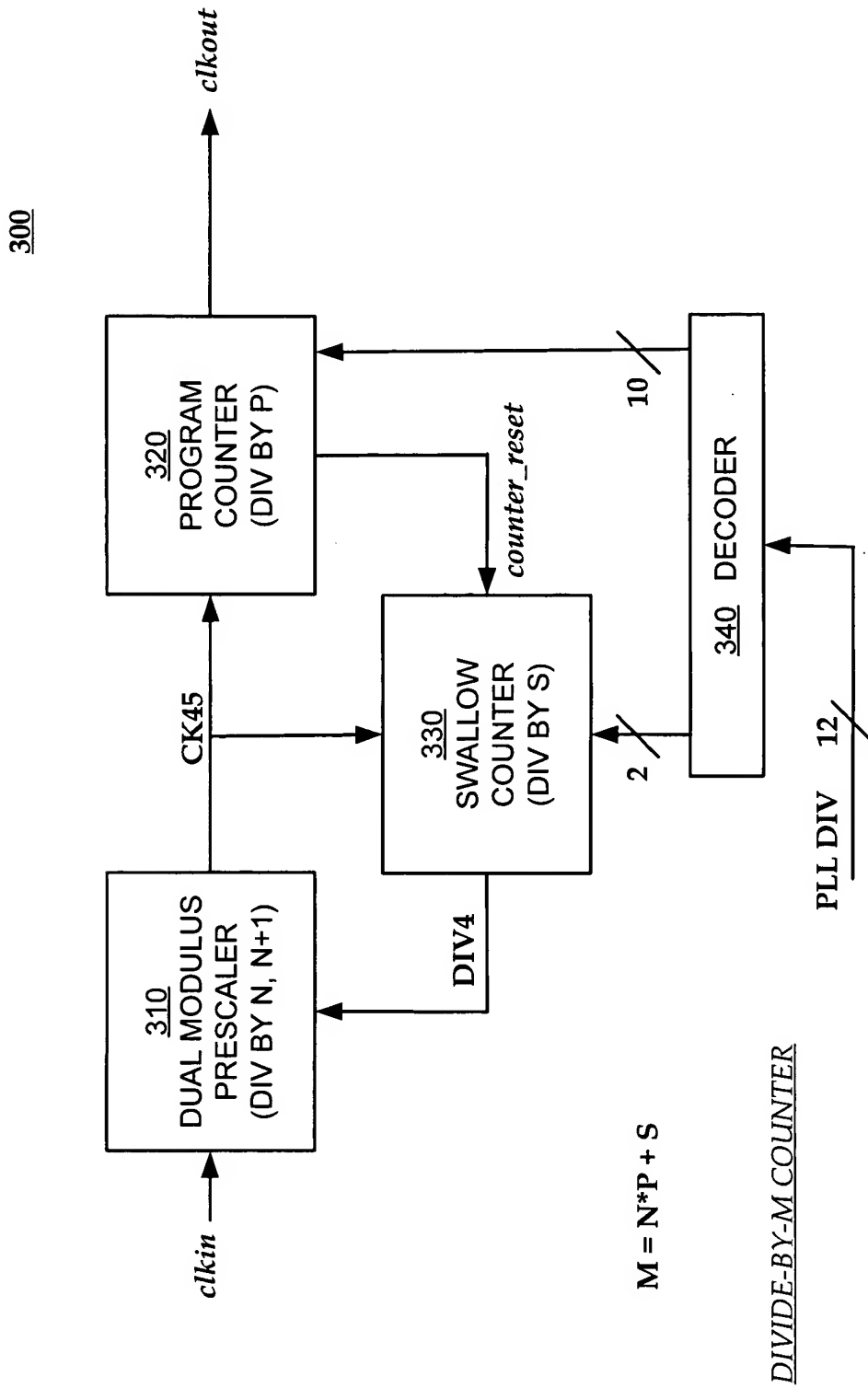


FIGURE 3

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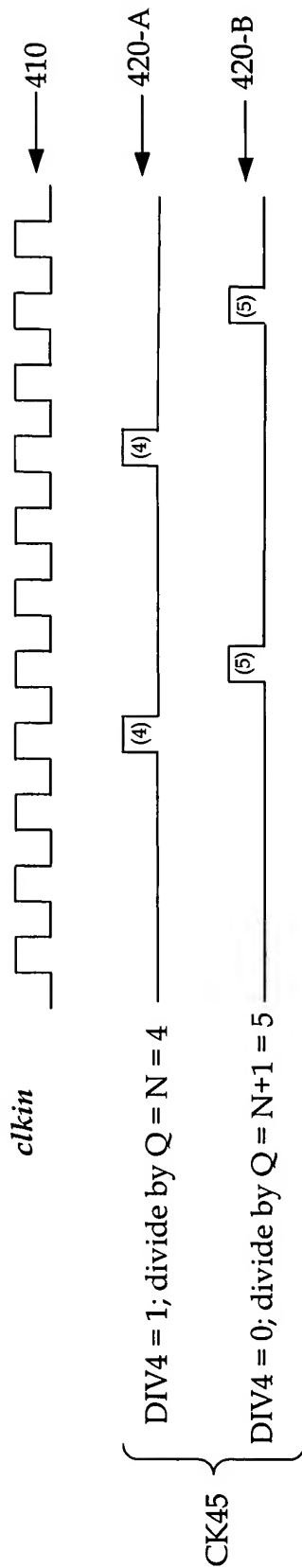


FIGURE 4A

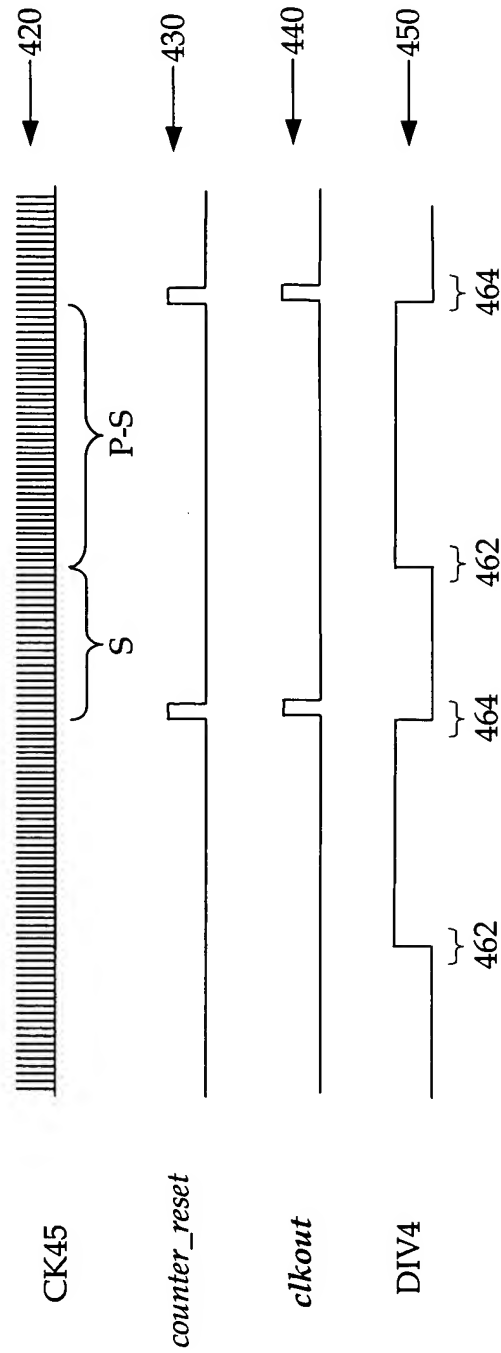


FIGURE 4B

500

$M = N * P + S$

FOR N=4

M (12 bit)	DIV ← M-1 (12bit)	P ← DIV[11:2] (10 bit)	S ← DIV[1:0] (2 bit)
(values)		(values)	(values)
17-20	...	4	0-3
21-24		5	0-3
25-28		6	0-3
29-32		7	0-3
33-36		8	0-3
37-40		9	0-3
...		...	
1009-1013		252	0-3
...		...	
2033-2036		508	0-3
...		...	
3073-3076		768	0-3
...		...	
4093-4096		1023	0-3

FIGURE 5

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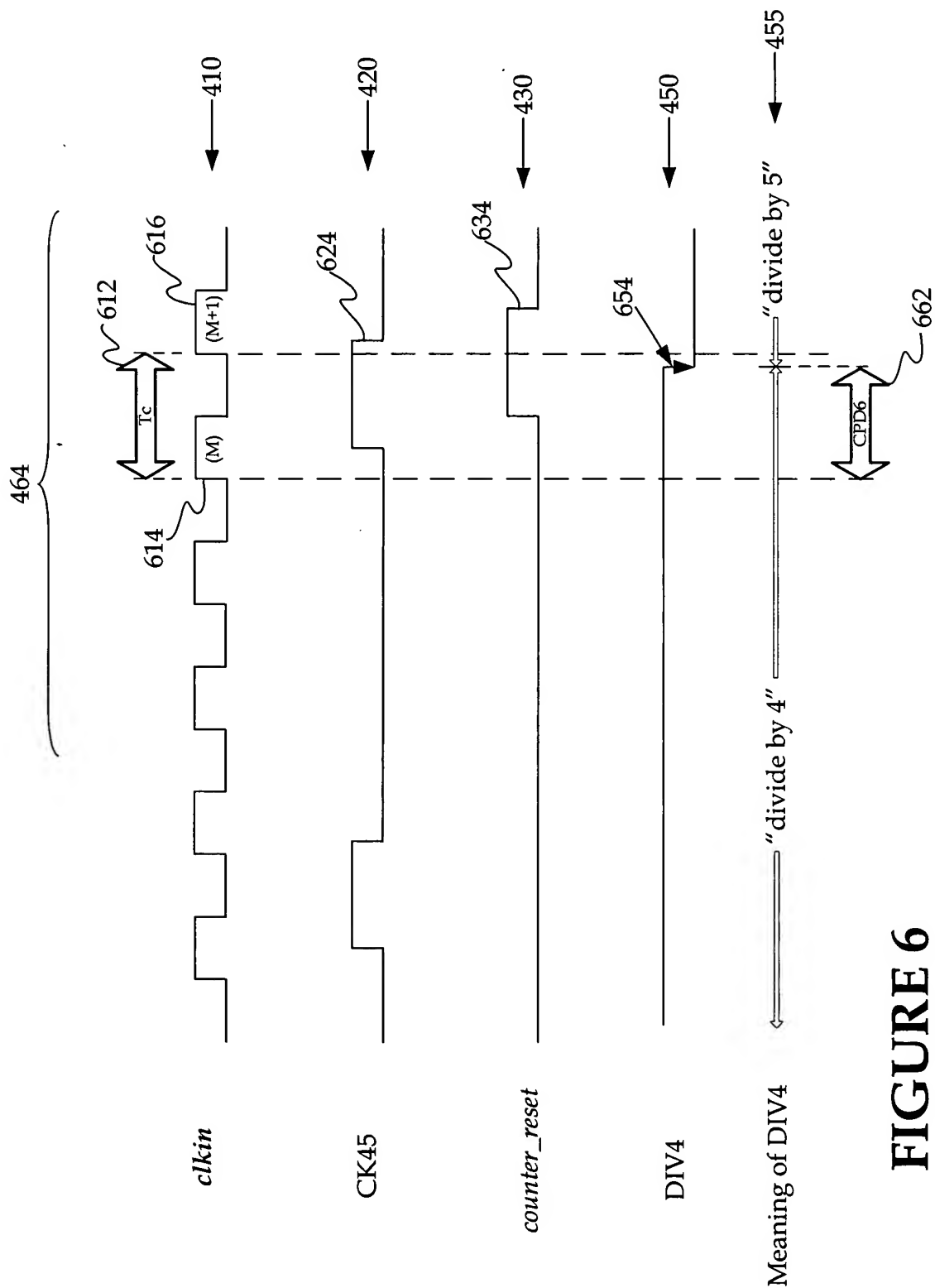


FIGURE 6

700

N = 4

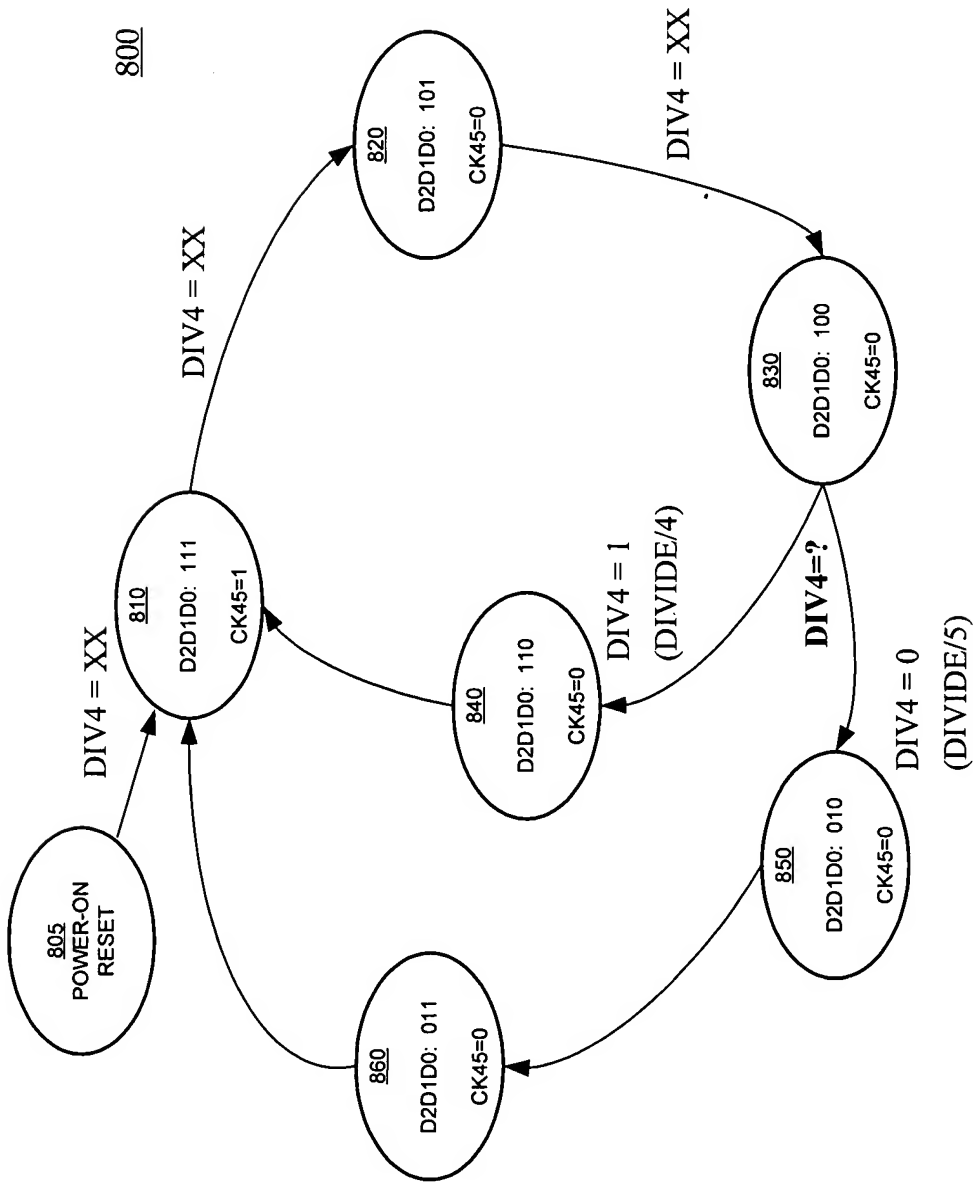
VARIABLE TYPE	SYMBOL	START (AT POR)	NEXT ASSIGNED VALUE
INTERNAL	D2	1	NEXT_D2 = DIV4 OR D0
INTERNAL	D1	1	NEXT_D1 = ~(D2 AND D0)
INTERNAL	D0	1	NEXT_D0 = D1
OUTPUT	CK45	1	NEXT_CL45 = D2 AND D1 AND D0

PRESCALER LOGIC

XX = DON'T CARE

FIGURE 7

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XX = DON'T CARE

PRESALER STATE MACHINE

FIGURE 8

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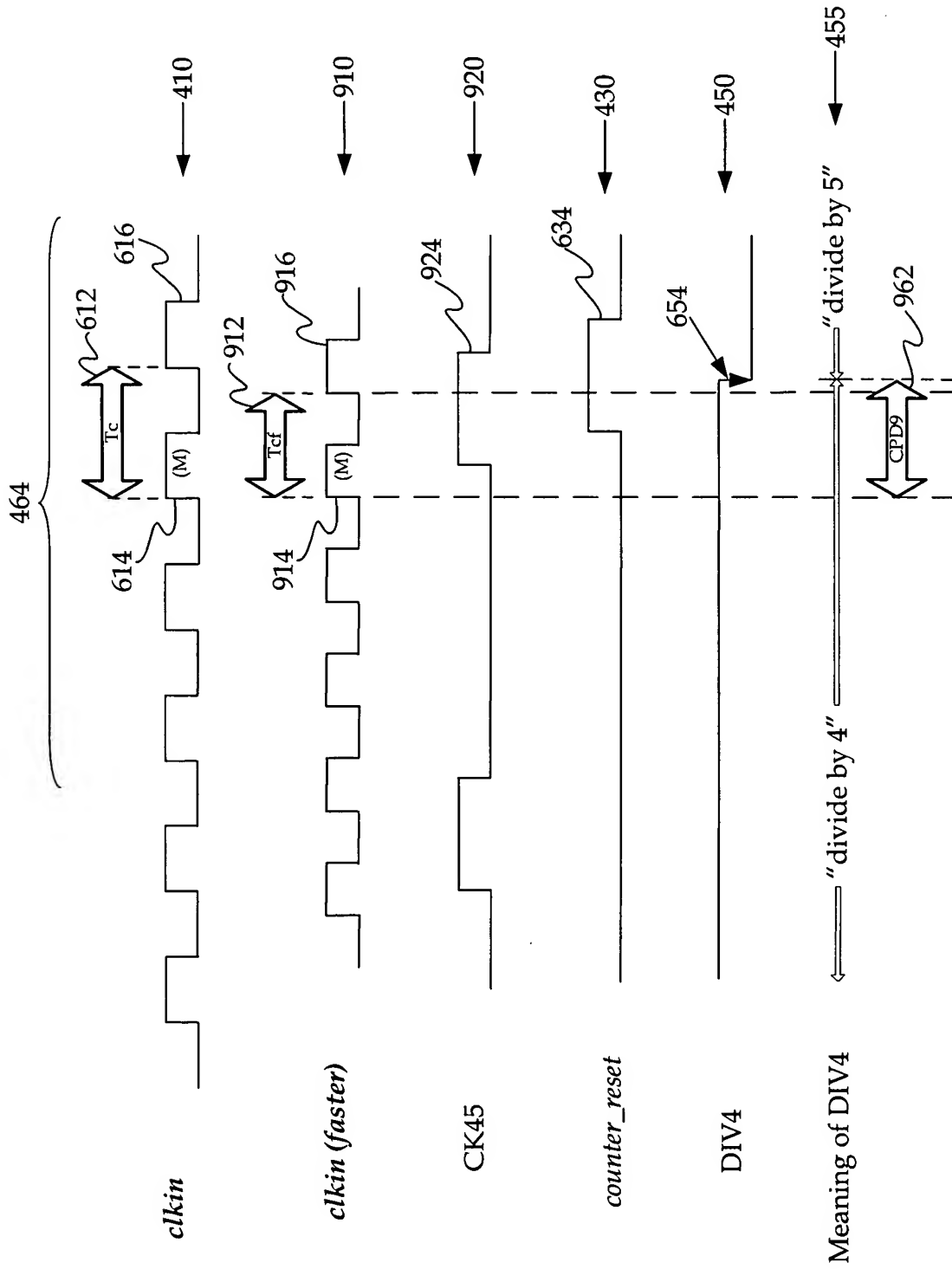


FIGURE 9

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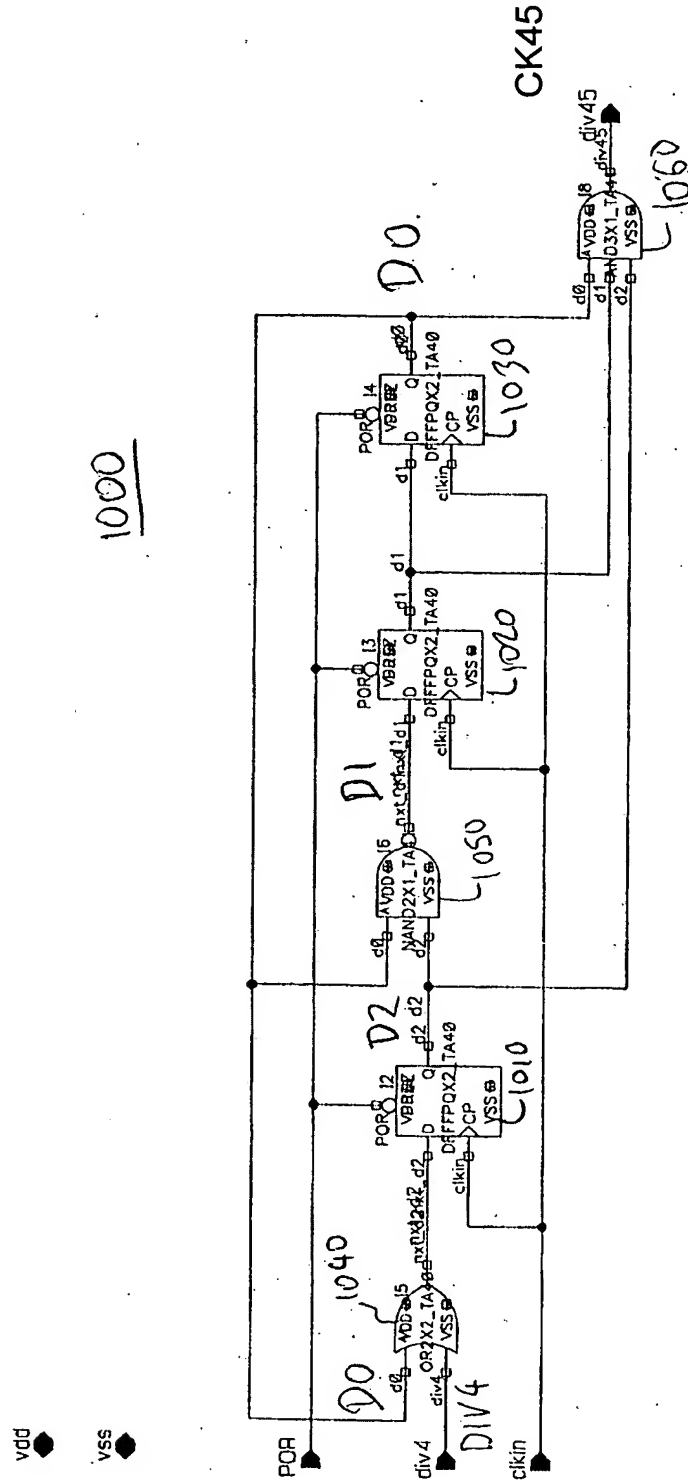
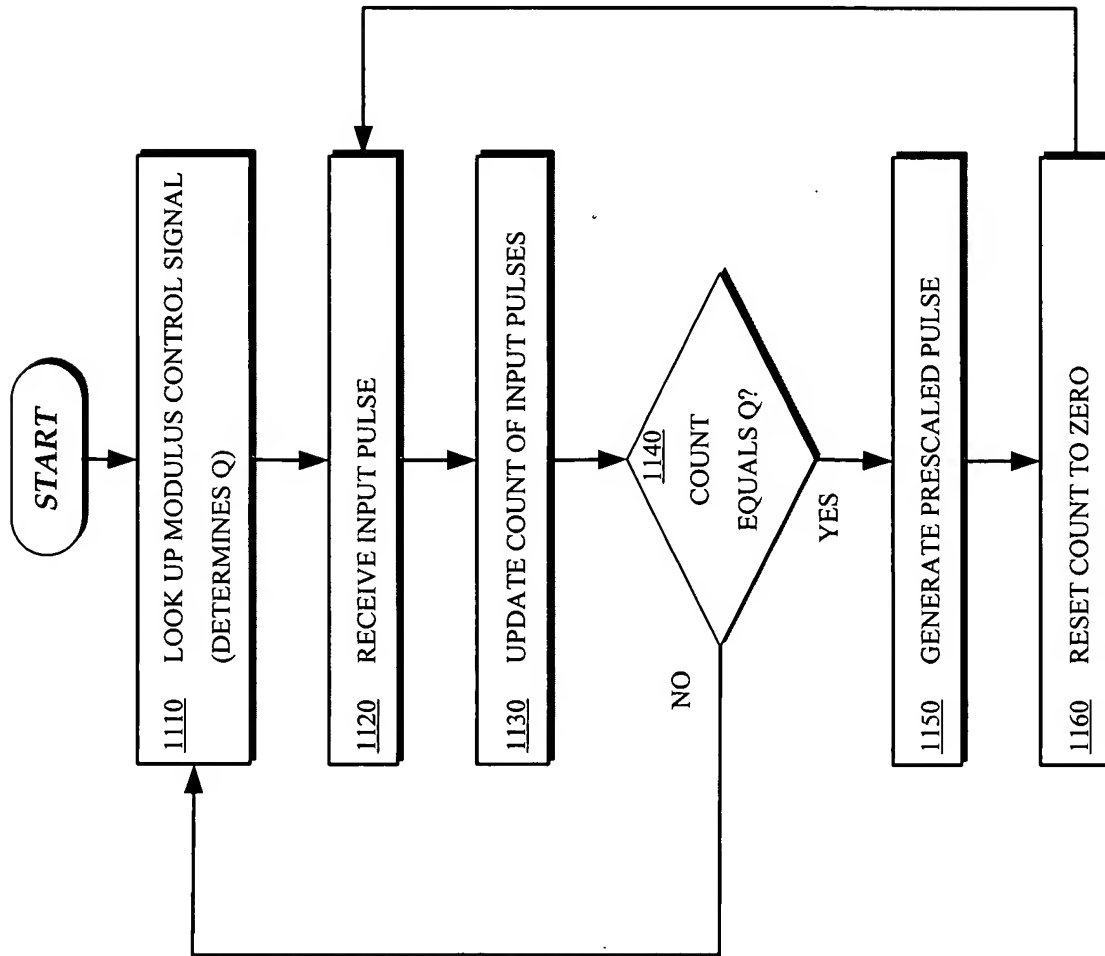


FIGURE 10

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1100

FIGURE 11